REMARKS AND ARGUMENTS

Objection to the Drawings

The drawings have been objected to by the Draftsperson as informal. Specifically, the margins in the drawings are not acceptable. Applicant, in response, have amended the drawings to comply with margins specified in 37 CFR 1.84(g). Applicants therefore submit that the objection to the drawings have been traversed.

Rejection under 35 USC §102

Claims 1-4, 13-15 and 17-18 are rejected under 35 USC § 102(b) as being anticipated by US Patent No. 5,844,856 (Taylor). Applicant respectfully disagrees.

Claim 1, by way of this response, has been amended to more clearly recite the invention. As amended, claim 1 recites an IC comprising a memory cell array having a plurality of memory cells, wherein the memory cells includes at least first and second ports forming a memory cell array with at least first and second access ports for accessing the memory cells. A cache memory is coupled to the first and second access ports, wherein during a read operation to the memory cell array to obtain read data through one of said first and second access ports, the cache memory provides the read data if the read data is contained therein or the memory cell array provides the read data if the read data is not contained in the cache memory. A refresh control circuit is provided for performing refresh operations.

Taylor describes dual port memories and systems. However, in contrast to the present invention, the memory cells described by Taylor are single port memory cells forming a single access port array. To provide a memory system with two ports, two arrays are provided, each with a single data port. See Taylor, Abstract and Fig. 1. Taylor nowhere teaches or suggests the use of memory cells with at least first and second ports to provide an

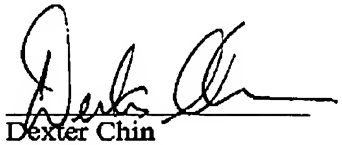
array with at least first and second access ports. As for 13 and 17, they have been amended to more clearly recite a memory array having memory cells with at least first and second ports to form a memory array with first and second access ports. Likewise, newly added claim 20 recites a memory array having memory cells with at least first and second ports to form a memory array with first and second access ports. Therefore, Applicant submits that claims 1, 13, 17 and 20 are patentable over Taylor. Since claims 2-12, 14-16, 18-19 and 21-25 are directly or indirectly dependent on claims 1, 13, 17 or 20, these claims are also patentable over Taylor.

Conclusion

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance and the issuance of a formal Notice of Allowance at an early date is respectfully requested. Should the Examiner believe that a telephone conference would expedite prosecution of this application, please telephone the undersigned attorney at his number set out below.

Date: February 07, 2005

Respectfully submitted,



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